DESIGN, IMPLEMENTATION AND CHARACTERIZATION OF XOR PHASE DETECTOR FOR DPLL IN 45 NM CMOS TECHNOLOGY

Delvadiya Harikrushna I[1], Prof. Mukesh Tiwari[2], Prof. Jay Karan Singh[3]
Dr. Anubhuti Khare[4]

[1]Department of Electronics &Communication, Sri Satya Sai Institute of Science & Technology
hkpatel13@gmail.com
[2,3]Professor, Department of Electronics &Communication
Sri Satya Sai Institute of Science & Technology
Sehore, Bhopal, Madhya Pradesh, India
Jksingh81@yahoo.co.in

[4]UIT, Rajiv Gandhi Proudhyugiki Vishwavidhyalaya University Bhopal, MP, India.

ABSTRACT

In this paper the implementation of XOR phase detector in 45 nm submicron CMOS technology and it's CMOS design layout using Microwind 3.1 for Digital Phase Locked Loop in sub-nanometres CMOS Technology is presented. The input-output transfer characteristic of XOR phase detector is presented. The CMOS XOR phase detector produces error pulses on both rising and falling edges while the CMOS phase frequency detector will respond only to positive or negative transitions. XOR phase detector will try to lock on both rising as well as falling edge while the PFD (phase frequency detector) will lock on either rising edge or falling edge of reference signal and feedback signal.

KEYWORDS

PLL, XOR Phase Detector, Phase Frequency Detector, CMOS layout design.

1. INTRODUCTION

A function of digital phase-locked loop is to lock to the phase of an input reference signal with the feedback signal produce by VCO and passes through divider circuitry. A basic form of a PLL consists of three fundamental blocks, namely,

- Phase detector (PD).
- Loop filter.
- Voltage controlled oscillator (VCO)

The phase detector compares the phase of input signal or reference signal with the phase of signal produced by the VCO. Phase detector compares the phase difference between two input signal and produce Output signal in form of difference voltage proportional to phase difference. The difference voltage signal is filtered by the loop filter and applied to the input to VCO(Vcontrol). The control voltage on the VCO produce the frequency such that reduces the phase difference between the input signal and the local oscillator. When the loop is locked, than

both signal's phase are equal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL.

2. PHASE DETECTOR

Generally two broad categories of phase detectors can be distinguished: multiplier circuits and sequential circuits. Multipliers generate the useful DC error output as the average product of the input-signal waveform times the local oscillator waveform. A properly designed multiplier is capable of operation on an input signal buried deeply in noise. A sequential phase detector generates an output voltage that is a function of the lime interval between a zero crossing on the signal and a zero crossing on the VCO waveform. Sequential phase detectors are capable of detecting both the phase and frequency differences [4]. There are two main digital phase detectors:

- XOR phase detector.
- Phase/frequency detector.

3. XOR PHASE DETECTOR

The XOR phase detector is simply exclusive OR gate. We know the simple operation of exclusive OR gate, it compare phase difference between both signal and produce output pulses basis on the input varies. It provide dc level proportional to the phase difference between the inputs. While the XOR circuit produces error pulses on both rising and falling edges. The operation of phase detectors is similar to that of differential amplifiers in that both sense the difference between the inputs, generating a proportional output. It doesn't contain any phase difference information.

The phase difference between the dclock and data is given by

$$\Delta\phi = \phi_{data} - \phi_{dclock} = \frac{\Delta t}{T_{dclock}} \cdot 2\pi(radians) \quad \text{.....(1)}$$

or, in terms of output clock frequency

$$\Delta\phi = \frac{\Delta t}{2T_{clock}} \cdot 2\pi \quad \text{.....(2)}$$

$$f_{clock} = \frac{1}{T_{clock}} = 2f_{dclock} = \frac{2}{T_{clock}} \quad \text{.....(3)}$$

When the loop is locked, the clock rising edge is centered on the data; the time difference, Δt, between the dclock rising edge and the beginning of the data is simply $T_{clock}/2$ or $T_{dclock}/4$ (Figure 1c). Therefore, the phase difference between dclock and the data, under locked conditions, may be written as

$$\Delta\phi = \frac{\pi}{2} \quad \text{.....(4)}$$

The average voltage out of the phase detector may be expressed by

$$V_{PDout} = VDD \cdot \frac{\Delta\phi}{\pi} = K_{PD} \cdot \overset{input}{\widetilde{\Delta\phi}} \quad \text{.....(5)}$$

where the gain of the PD may be written as

$$K_{PD} = \frac{VDD}{\pi}(V / radians) \quad \text{.....(6)}$$

To understand how the phase detector works, see diagrams shown in fig 1. If the data signal and clock signal edges start and stop at same time, (figure 1a), phase difference is zero hence the XOR output, V_{PDout}, is 0V. As shown in figure 1b & 1c, the phase difference is $3\pi/4$ and $\pi/2$.

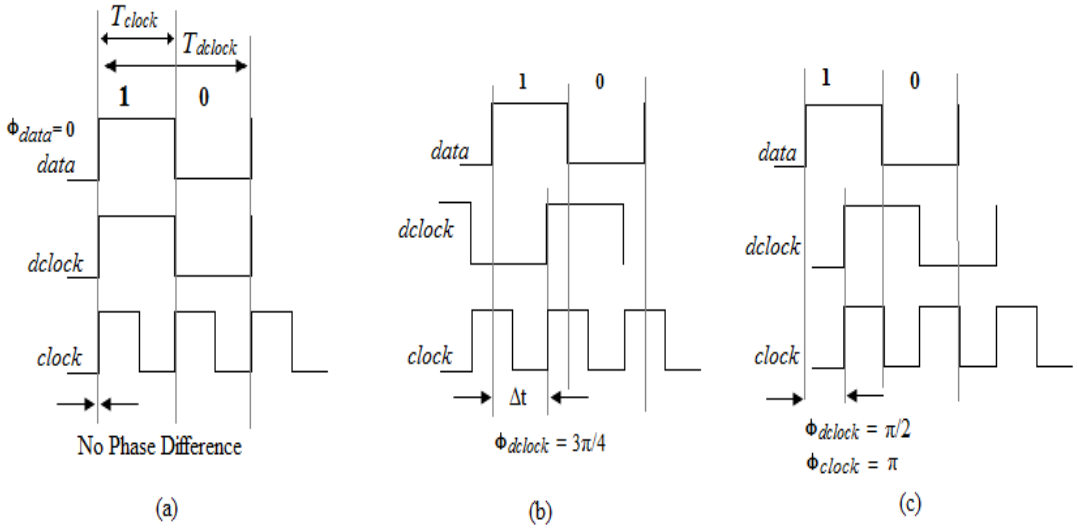

Figure 1. XOR PD output for various inputs

As shown in figure 1 the implementation of XOR Phase Detector in sub- nanometer CMOS technology which is used in PLL to lock the phase of the feedback signals with reference clock signal. The figure 2,3,4,5,6,7,8,9,10,11,12,13,14,15,16 shows the implementation, simulation results, characterization and detailed analysis of the XOR PD when the reference and feedback signals are out of phase by zero, π/2, π, 3π/2, 2π respectively. Here we consider feedback signal dclock signal is leading with respect to data signal and vice-versa, we get the final characteristic as plotted in figure 17.

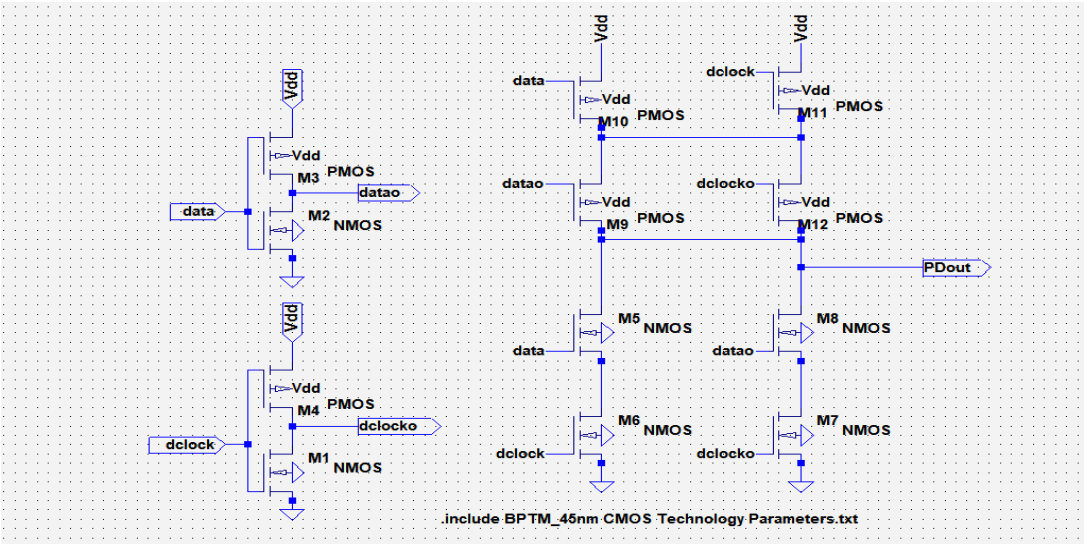

Figure 2. Implementation of CMOS XOR Phase Detector

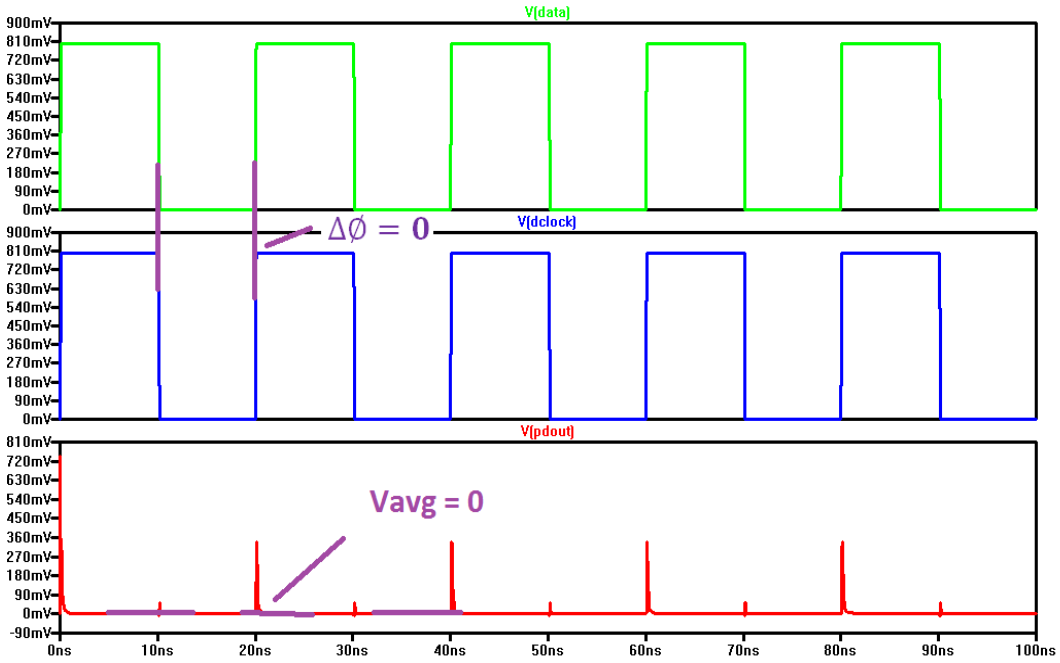

Figure 3. XOR Phase Detector with Phase Difference = 0

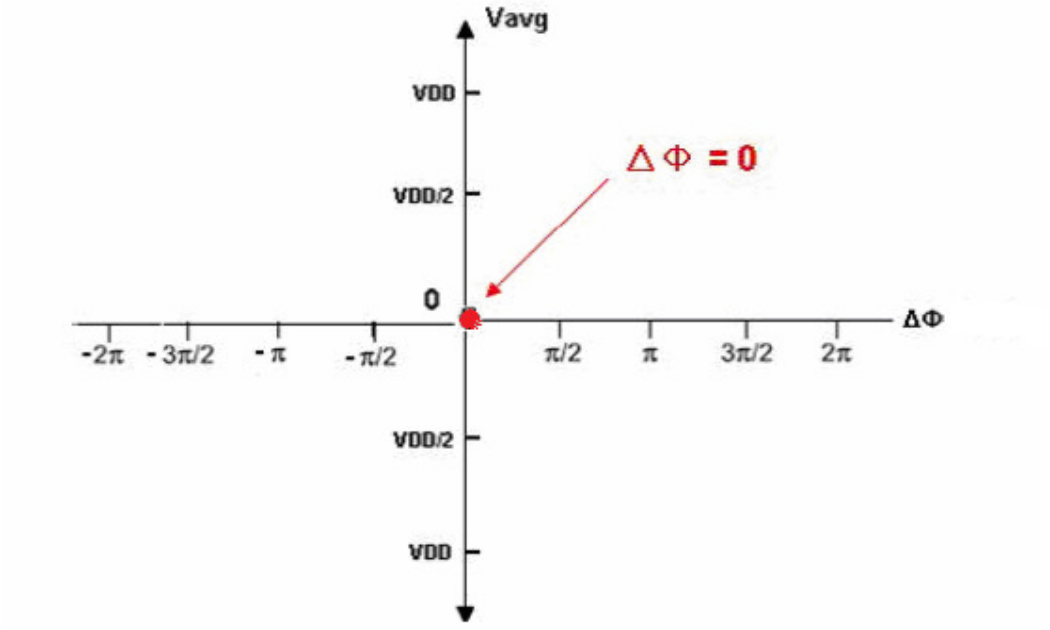

Figure 4. Characterization of XOR Phase Detector with Phase Difference = 0

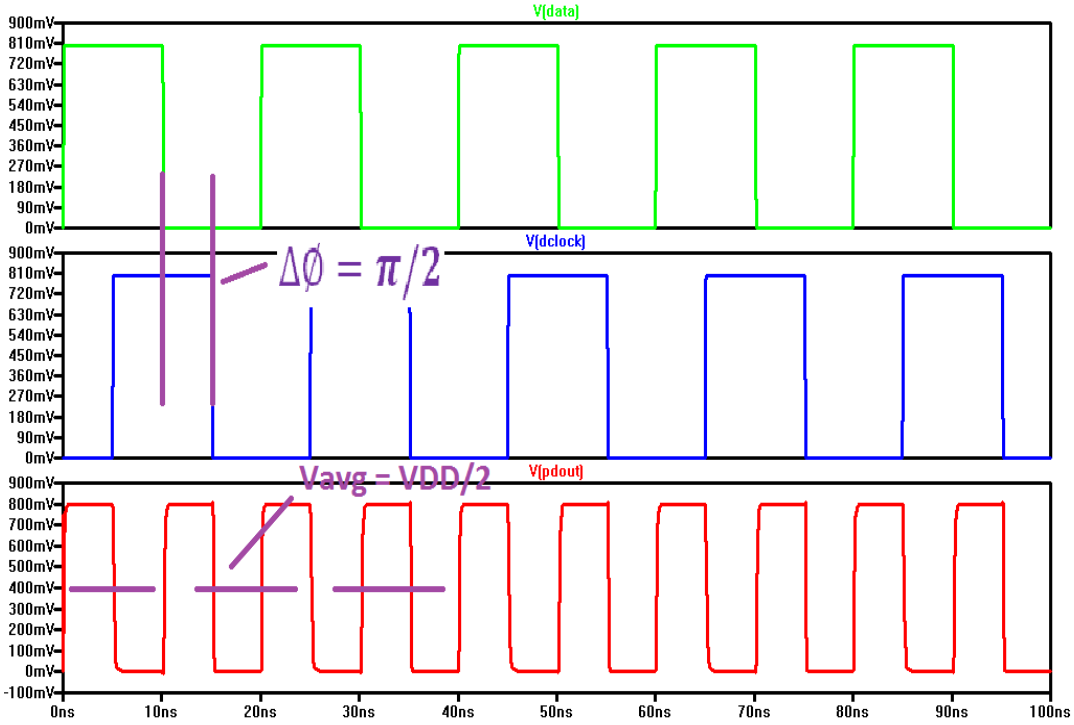

Figure 5. XOR Phase Detector with Phase Difference = π/2 (when dclock leads data by π/2)

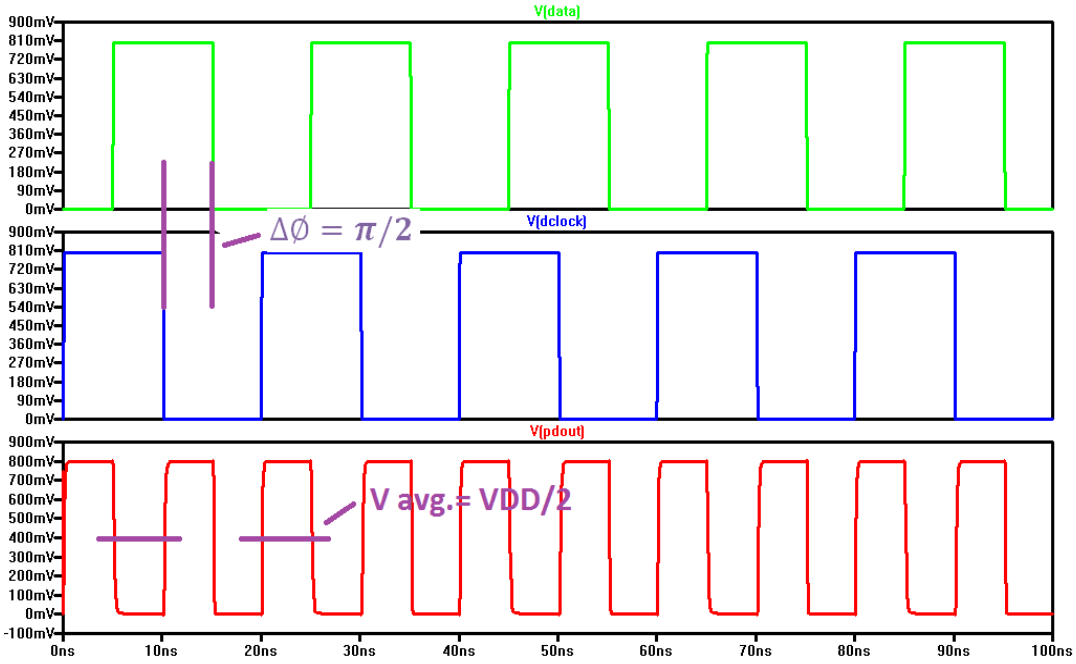

Figure 6. XOR Phase Detector with Phase Difference = π/2 (when data leads dclock by π/2)

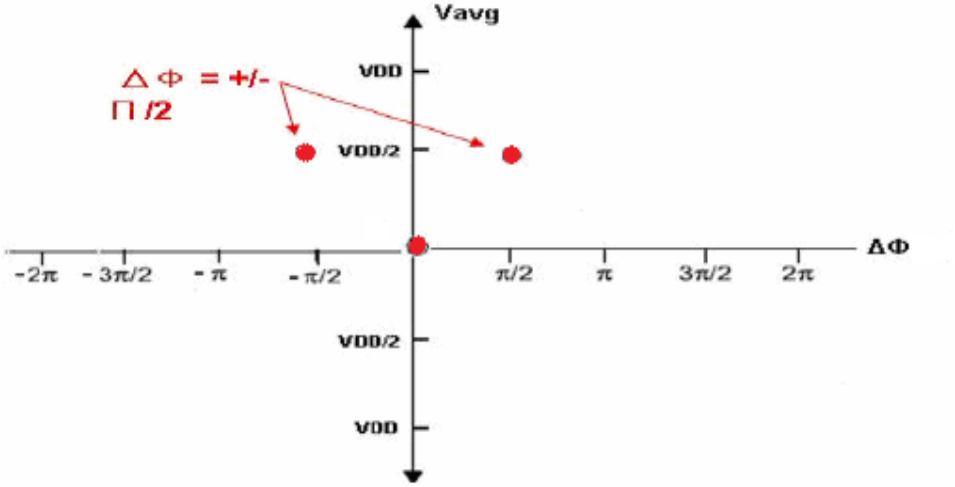

Figure 7. Characterization of XOR Phase Detector with Phase Difference = π/2

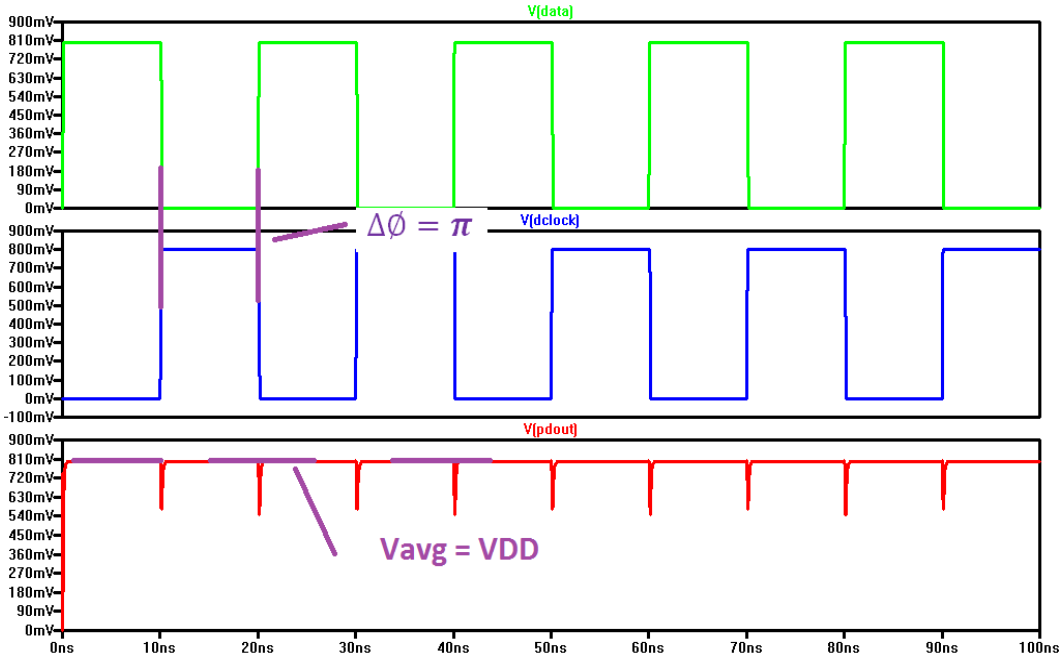

Figure 8. XOR Phase Detector with Phase Difference = π (when dclock leads data by π)

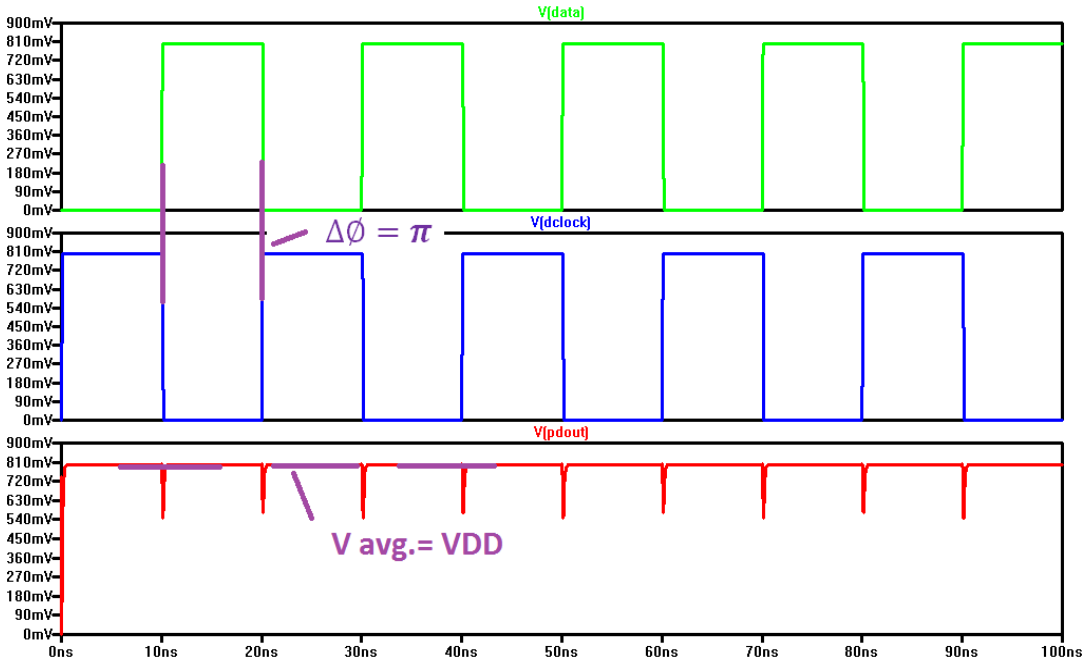

Figure 9. XOR Phase Detector with Phase Difference = π (when data leads dclock by π)

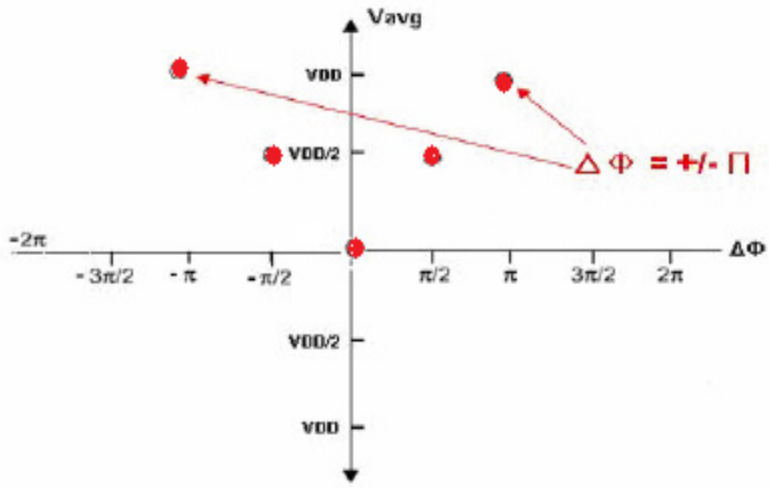

Figure 10. Characterization of XOR Phase Detector with Phase Difference = π

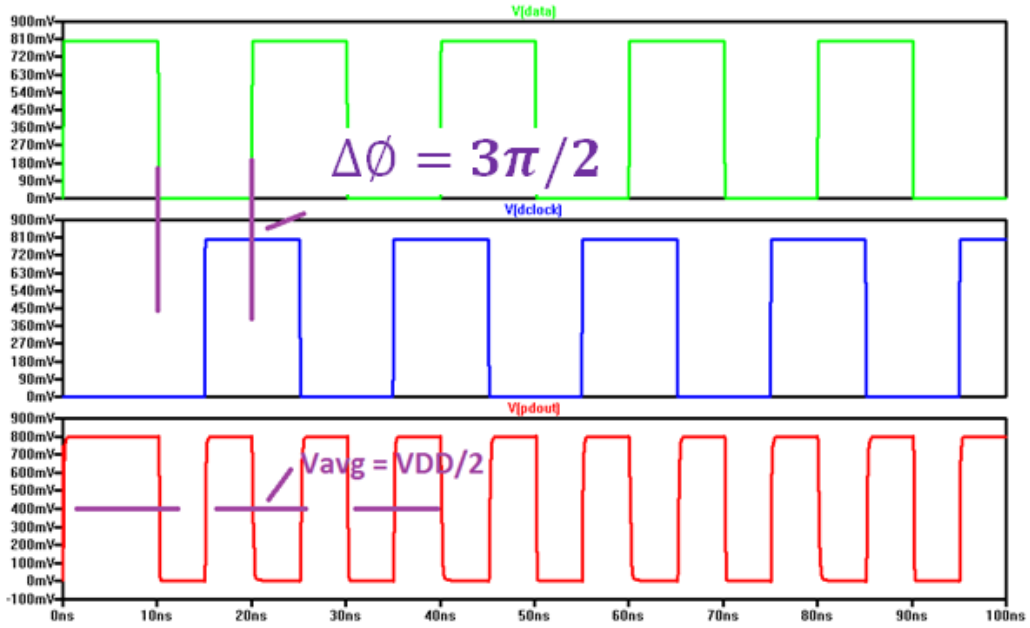

Figure 11. XOR Phase Detector with Phase Difference = 3π/2 (when dclock leads data by 3π/2)

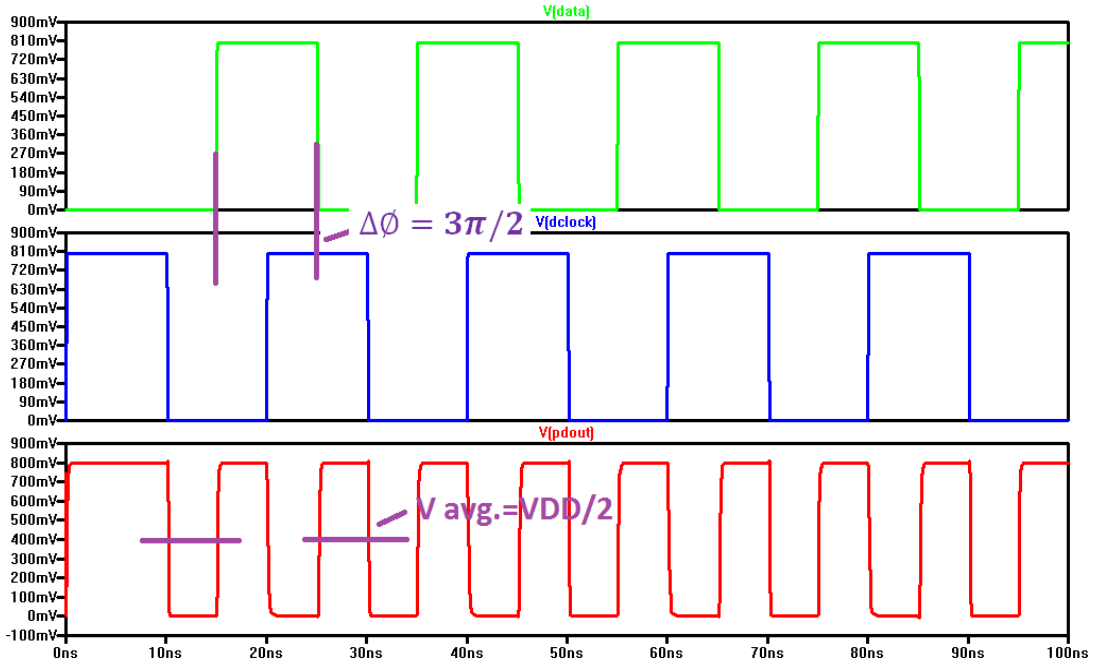

Figure 12. XOR Phase Detector with Phase Difference = 3π/2 (when data leads dclock by 3π/2)

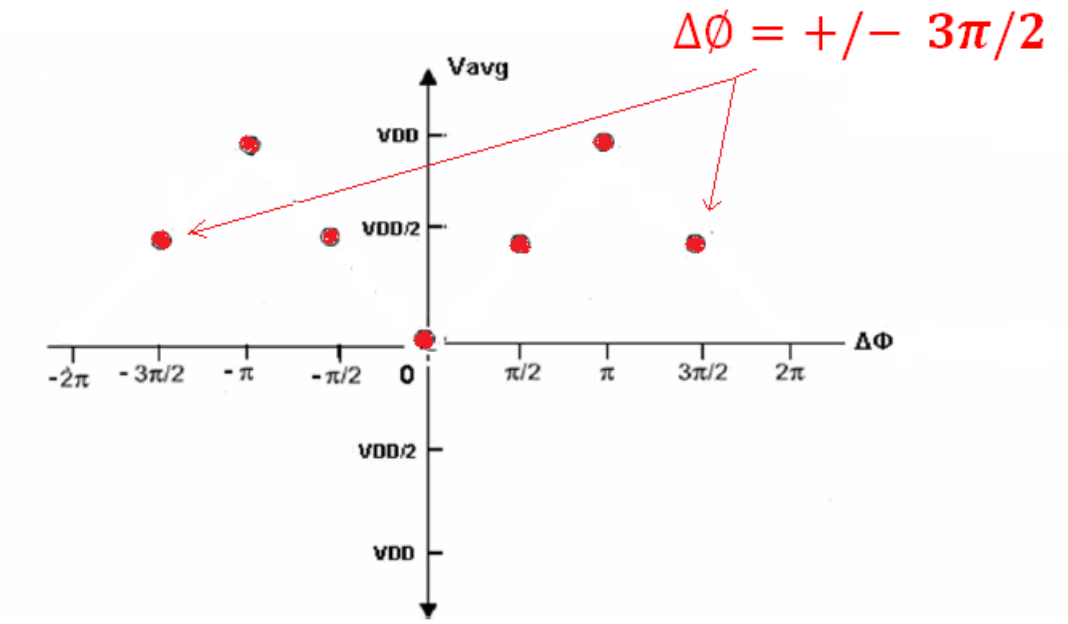

Figure 13. Characterization of XOR Phase Detector with Phase Difference = 3π/2

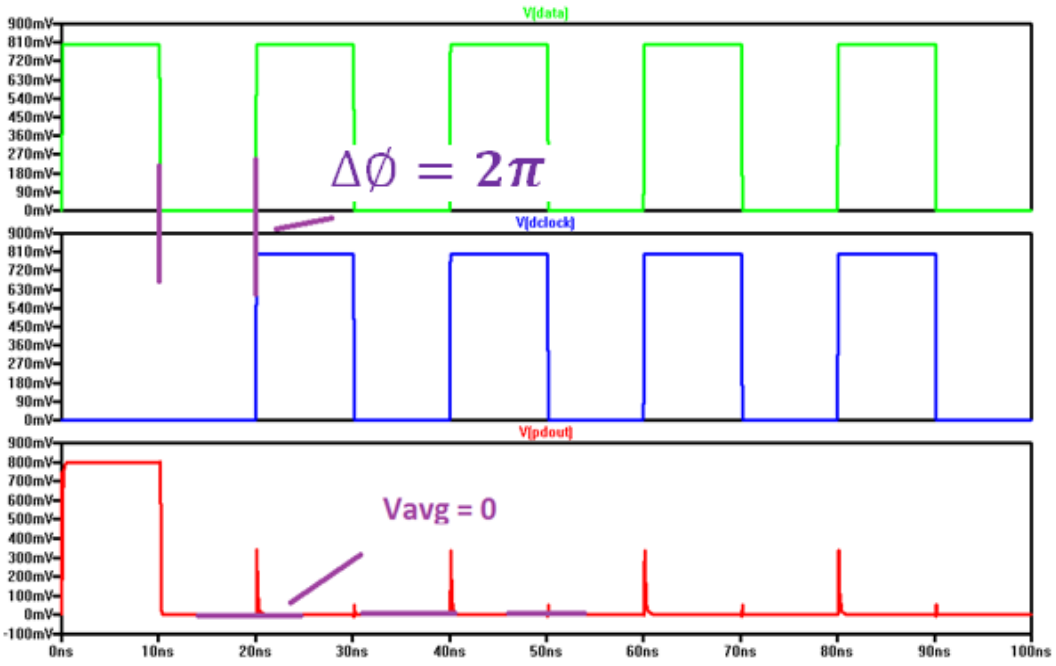

Figure 14. XOR Phase Detector with Phase Difference = 2π (when dclock leads data by 2π)

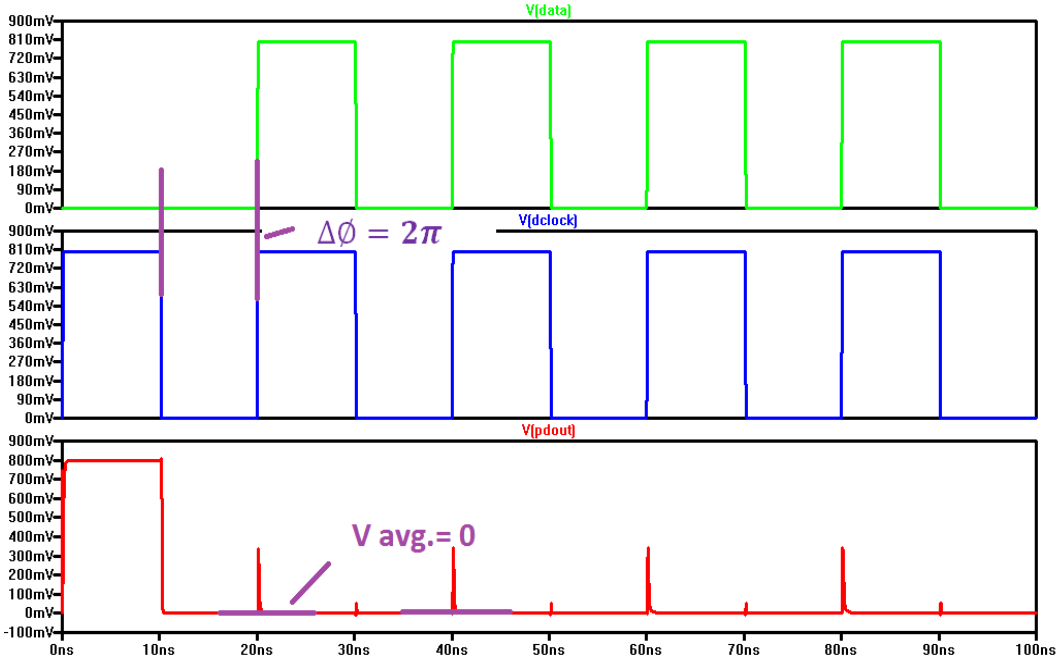

Figure 15. XOR Phase Detector with Phase Difference = 2π (when data leads dclock by 2π)

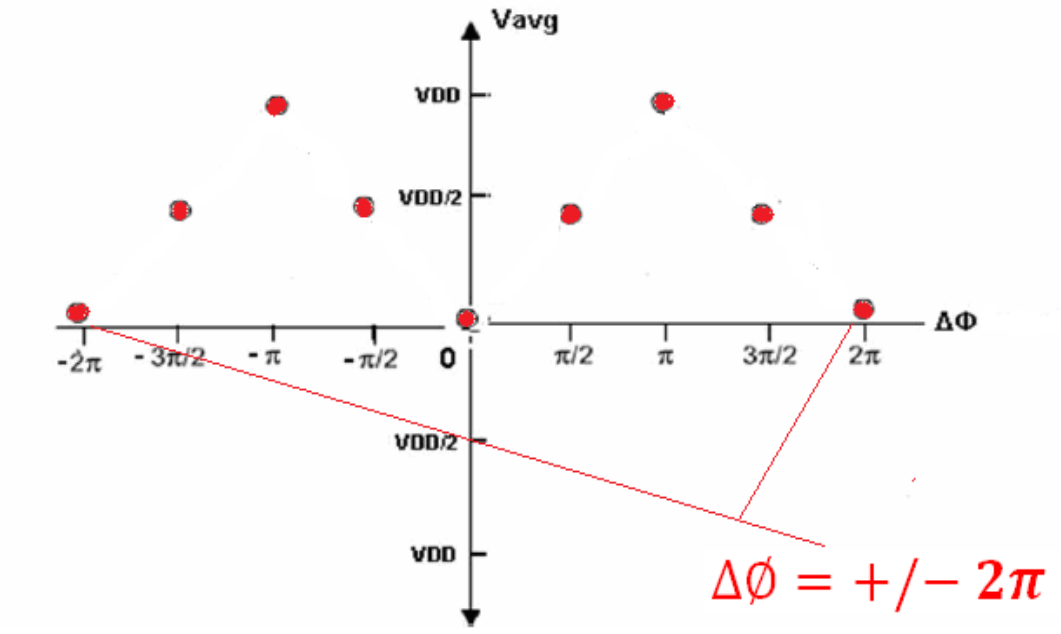

Figure 16. Characterization of XOR Phase Detector with Phase Difference = 2π

The XORPD input/output transfer characteristic graph is a plot of average output voltage V_{avg} versus the phase difference $\Delta\Phi$. The XOR PD characteristic plot is shown in figure 17. As

shown in figure 17, when the reference clock signal is delayed with respect to feedback signal, the phase difference $\Delta\Phi$ becomes negative and we get same average voltage V_{avg} that we have got when the feedback signal was delayed by zero, π/2, π, 3π/2, 2π with respect to the reference clock signal.

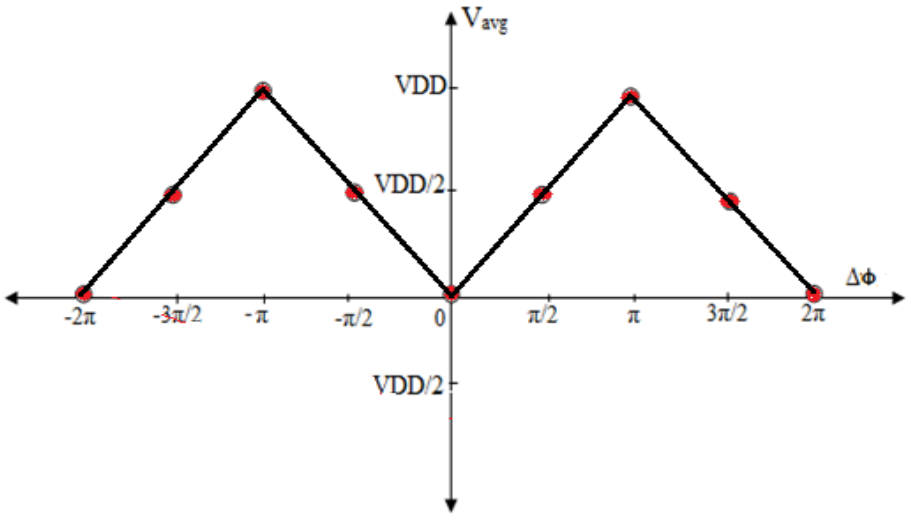

Figure 17. Input/output transfer characteristic of CMOS XOR Phase Detector

4. CMOS LAYOUT DESIGN

We have observed the implementation of XOR phase detector now see below figure 18 & 19 shows the CMOS layout design for the XOR phase detector simply verified truth table of the XOR gate or we can say it detect when there is any change in it's input phase.

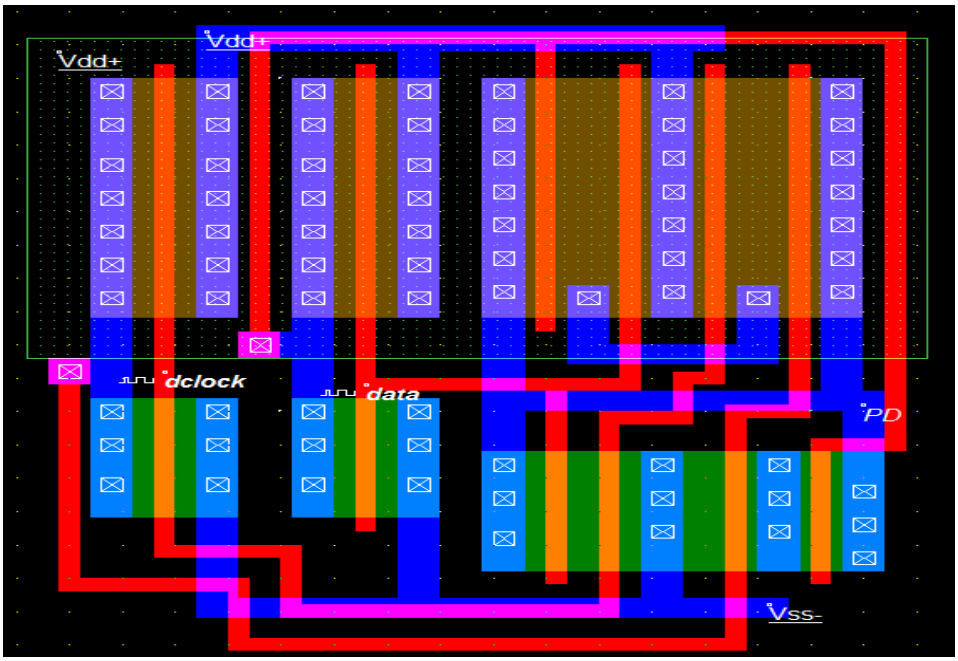

Figure 18. CMOS design layout of XOR phase detector

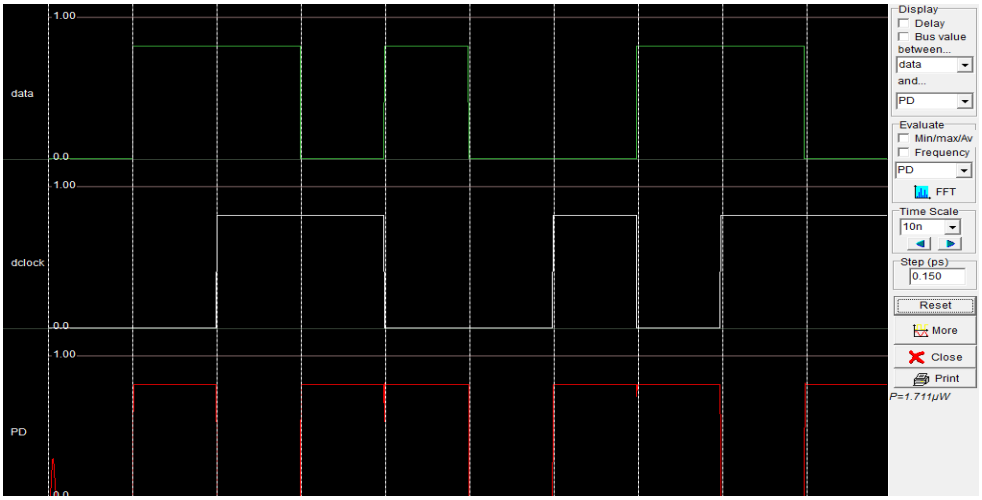

Figure 19. Output result of XOR phase detector

5. CONCLUSION

The major disadvantage of XOR Phase Detector is that it can lock onto harmonics of the reference clock signal and most importantly it cannot detect a difference in frequency. To take care of these disadvantages, we have implemented the Phase Frequency Detector, which can detect a difference in phase and frequency between the reference clock signal and feedback signals.

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H. I. Delvadiya. A PG Student form Shree SatyaSai Institute Of Science & Technology, Sehore, Bhopal, MP. He is Completed BE in Electronics & Communication (EC) from V.V.P. Engg. College Rajkot, Gujarat in 2008, DE (EC) from A.V.P.T.I. Rajkot, Gujarat in 2005. His area of interest is VLSI Technology and Embedded System & Wireless Communication.

Prof. Mukesh Tiwari. He had completed M.Tech from RGPV university, Bhopal, MP, India. He is working as Director of institute & professor at department of Electronics and Communication at Shree Satya Sai Institute of Science and Technology, Sehore, Bhopal, MP. His area of interest is Wireless Communication, VLSI Design.

Prof. Jay Karan Singh. He is Research scholar Electronics and Communication in RGPV University, Bhopal. He had completed M.Tech in Microelectronics and VLSI design in 2009 from RGPV university, Bhopal. He is working as Professor and Head of department of Electronics and Communication at Shree Satya Sai Institute of Science and Technology, Sehore, Bhopal, MP. His area of interest is Wireless Communication, Microelectronics', VLSI Design.