ALL DIGITAL WIDE RANGE MSAR CONTROLLED DUTY-CYCLE CORRECTOR

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ABSTRACT

A clock with 50% duty cycle is very significant in many applications such as DDR-SDRAMs and double sampling analog-to-digital converters. This crisp presents a Modified Successive Approximation Register (MSAR) controlled duty cycle corrector (DCC), to attain 50% duty cycle correction. Here MSAR adopts a binary search method to compress lock time while maintaining tight synchronization between effort and production clocks. The MSAR-DCC circuit has been implemented in a 0.18- µm CMOS process which corrects the duty rate within 5 cycles which has a closed loop characteristics. The measured power dissipation and area occupation are 5581nW and 0.033mm^2 respectively.

KEYWORDS

Duty Cycle, Duty cycle corrector (DCC), Double data rate (DDR), Successive Approximation Register (SAR), Modified Successive Approximation Register (MSAR), PVTL.

1. INTRODUCTION

The preponderance numerous clock signal is in the form of a square wave with a 50% duty cycle. Circuits using the clock signal for bringing together may become dynamic at either the upward edge, downward edge, or, in the case of double data rate, together in the rising and in the declining limits of the clock cycle.

A clock with 50% duty cycle is vital factor in various applications such as DDR-SDRAMs and twice sampling ADCs. To twice the data rate, mutually positive and negative transition edges of a clock are used. However, the duty-cycle alteration of a clock occurs owing to the unmatched rising time and falling time in the clocking paths. Therefore, the duty cycle of clock signal is intricate to fix at 50%. Since improving the speed of computer systems demands low-power high-speed memory such as DDR3 and promising DDR4 DRAMs, it has become more important to develop a low-power high-performance DCC.

The main objective of this work is to achieve 50% duty cycle in order to avoid corrupt data transmission caused by inappropriate data windows, leading to data rate reduction. Many duty cycle alignment circuits have been developed to solve the duty cycle distortion (DCD) of the clock, such as a duty cycle corrector (DCC).

2. RELATED WORKS

There are two categories to recognize the DCC in novel: the feedback type and non feedback one. The non-feedback digital DCCs have the benefits of fast duty-correction and low-power operation. However, the DCCs utilizing interruption have speed restrictions on the maximum

operation frequency and the open-loop characteristic cannot trail the process, voltage and temperature (PVT) variations. The analog-feedback DCCs usually implement the negative feedback scheme which achieves higher duty cycle accuracy but it leads to long duty-correction time.

The non-feedback digital DCCs have the profits of fast duty-correction and low-power operation and its open-loop characteristic cannot follow the process, voltage and temperature (PVT) variations. To balance this PVT variation, it needs complex calibration and trimming circuitry, which increases the area over- head.

All digital-feedback DCCs can exact the 50% duty-cycle within the very short duty-correction time. However, DCCs uses complicated duty-cycle detector structures such as a time-to-digital converter (TDC)-based detector, which increases the overheads of hardware implementation and the performance of TDC such as the linearity can degrade the complete DCC performance.

In this crisp DCC has been implemented by using SAR and MSAR. In that, this predictable SAR stops their operation when its binary search operation has been completed. Thus the SAR-DCC becomes open loop and seriously exaggerated by PVTL variations. To overcome this shortcoming, conventional SAR has been replaced by modified SAR, which automatically enters into a counter mode after its binary search operation has been terminated.

This brief is organized as follows. In Section II, the architecture and operation of the SAR-DCC circuit are described. Also, the effectiveness of first exploiting the MSAR controller in the DCC circuit is discussed. Section III describes details of the implemented circuit. Section IV shows the results and discussions of the proposed circuit. Finally, the brief is concluded in Section V.

3. EXISITING WORK

3.1. SAR-DCC

Fig.1. shows the block illustration of SAR-DCC circuit, which comprises duty-cycle detector, a duty-cycle adjuster, its controller and an output buffer. The exploited SAR controller, which adopts the binary search algorithm, controls the duty-cycle adjuster to exact the clock duty-cycle by 50%. The duty-cycle detector in this concise just checks whether or not the positive duty-rate D_{OUT} is higher than 50%. It can be called “a duty-rate comparator”.

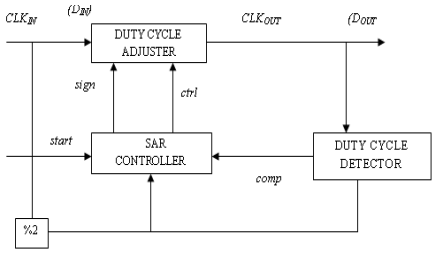

Figure 1. Block Diagram of the SAR-DCC

When the indicator *Start* goes to HIGH, the duty-cycle correction begins with initializing the control signals of the duty-cycle adjuster. All bits of the SAR control word *Ctrl* are set to LOW. The duty-rate comparing bit *Sign* of the input clock CLK_{IN} is determined by the signal *Comp*, which is the output signal of the duty-cycle detector in the case of no duty-cycle correction of

CLK_{IN}. The single-minded *Sign* contains the information about whether the duty-cycle adjuster increases or decreases the duty-rate of the output clock. After CLK_{IN} this determination, the duty-cycle correction is executed according to the binary search algorithm of the successive approximation. The sequential addition and subtraction of the binary-weighted duty-rate by *Ctrl* values, which is determined via the sequential values of *Comp*, adjusts the duty-cycle of CLK_{OUT} to 50%.

Finally, the signal *End* goes to HIGH, which can provide the finish information of the duty-cycle correction to the delay locked-loop (DLL) in DDR DRAMs. The effort of using bit *Sign* is to diminish the chip area of the duty-cycle adjuster by sinking the duty-cycle correction elements of the delay-lines.

3.1.1. Duty-Cycle Adjuster

Fig.2. shows a building block of duty-cycle adjuster. The adjuster consists of a variable falling edge generator with 6-bit programmable delay lines, fixed rising edge generator with dummy delay lines, latch, and MUX. The falling edge generator performs the duty-rate adjustment with the non-inverted or inverted signal CK_{IN} of the input clock CLK_{IN} by MUX selection and 6-bit control signals Ctrl[5:0] of the programmable delay line.

The earlier delay-line based duty-cycle adjuster circuit uses falling edge generators or both rising and falling edge generators for the duty-rate adjustment. Since a lower frequency operation is also required in DDR DRAM applications, the delay lines of the previous correction circuits are enlarged. In order to decrease delay lines, we employ only a falling edge generator with the input inversion MUX for duty-rate adjustment.

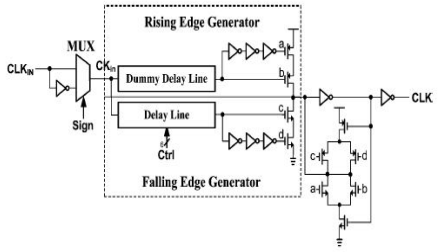

Figure 2.Duty Cycle Adjuster

At the first period of the duty-correction, there is no duty-rate change for the *Sign* determination of the input clock duty-cycle. The main drawback of this adjuster may be that the DLL requires a specially designed phase detector that selectively compares the rising and falling edges according to the control signal *Sign* from the DCC, which results in a complicated DLL design.

3.1.2. Duty-Cycle Detector

The duty-cycle detector of the duty-rate comparator comprises an analog amplifier of the logic amplifier, regenerative latch and inverter buffers as exposed in Fig. 3.

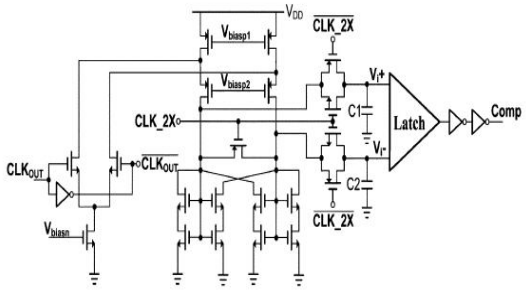

Figure 3.Duty Cycle Detector

The first folded preamplifier converts the differential clock signals into differential current signals and amplifies the current difference, which is incorporated into the capacitors C1 and C2. The second differential latch amplifies the integrated voltage difference to a full swing digital signal. Since the duty-rate comparator operates at high speed, the first stage of the preamplifier requires large bandwidth. The bias voltages are outwardly calibrated in order to reduce the mismatch of the integrated current and offset of the latch over the process variation.

3.1.3. SAR-Controller

Fig. 4 shows a 6-bit SAR block diagram with an added *Sign* register, which uses one of the most solid SARs with small chip area. The SAR determines the value of each bit of the control word *Sign* and *Ctrl* according to the sequential binary search based on the output of the duty-rate comparator *Comp*. The customized start circuit with the divided-by-2 clock *CLK_2X*, start signal *Start* and *Sign* bit is exposed. After the duty-cycle correction of the LSB determination in the SAR registers, this SAR circuit gives the in turn *End* of the correction finish, which goes to HIGH after determining ctrl[0]. The digitally stored data in SAR can support the power-down mode for the DDR DRAMs.

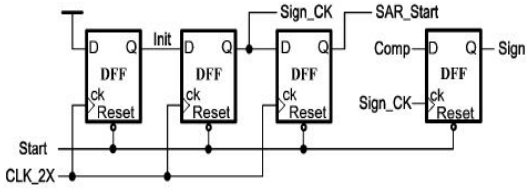

Figure 4.SAR controller with sign determination

4. PROPOSED WORK

4.1. MSAR-DCC

The operation of MSAR-DCC is similar to that of SAR-DCC but SAR-DCC is replaced by MSAR-DCC. The remaining blocks have been explained in previous section 3.1.1 and 3.1.2. The block diagram of MSAR-DCC circuit is revealed in Fig.5. this includes a duty-cycle detector, a duty-cycle adjuster, and modified SAR controller. The MSAR controller, which adopts the binary search algorithm, controls the duty-cycle adjuster to correct the clock duty-cycle by 50%. When the *Start* signal goes to HIGH, the duty-cycle correction begins with initializing the control signals of the duty-cycle adjuster.

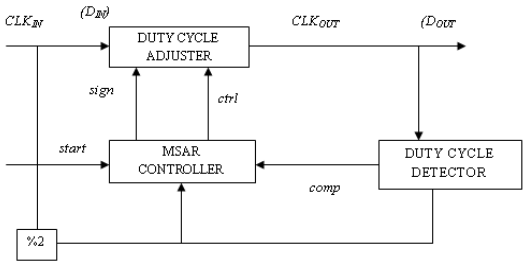

Figure 5. Block Diagram of the MSAR-DCC

Initially the duty cycle adjuster does not execute any operation. It passes input as output. Duty cycle detector detects the duty rate of an output clock and checks whether the duty rate is larger or smaller than 50%. Based on that, it will produce output signal as *comp*. When the MSAR controller finished their binary search algorithm it will automatically enters into a counter mode. Therefore, closed loop operation has been accomplished. Finally, the signal *End* goes to HIGH, which provides the stop information of the duty-cycle correction to the delay locked-loop (DLL) in DDR DRAMs. The *Sign* bit is to decrease the chip area of the duty-cycle adjuster.

4.1.1. MSAR-Controller

The operation of SAR circuit stops when the binary search is completed. So, the DCC becomes open-loop and cannot pursue the PVT variations. To realize the closed-loop operation, we need an additional counter. For a 6-bit SAR controller, a 6-bit UP/DOWN counter is desirable. The hardware transparency is double. To achieve the closed-loop operation after the binary search, the MSAR circuit is proposed. The closed-loop operation can be accomplished by entering the MSAR controller into a counter after its binary search operation has been completed. The MSAR unit is identical to a predictable SAR unit when the signal Enable is logic 0 and becomes a counter unit when the signal Enable is logic 1. Fig.6 reveals the realization of the MSAR unit.

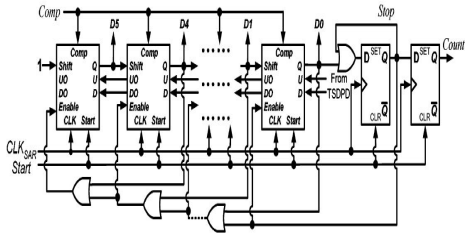

Figure. 6. 6-bit MSAR circuit

The 6-bit MSAR circuit consists of six MSAR units, two DFFs, and six OR gates, which is shown in Fig. 6. After that than the signal arises, the MSAR circuit is in the binary searching mode when the signal is logic 0. The signal decides the output of every SAR unit from the MSB to the LSB. Whereas the next MSAR unit performs the binary searching, the output throughout the OR gate arises and becomes the signal of the earlier MSAR unit to latch the determined value. At the same time, the preceding SAR unit is converted into a counter unit and starts to receive the outputs generated by the logic gates. The carry-out signals and for the counter mode are produced by the logic gates as fine. After the six-digit binary searching is finished, the signal arises to make sure that each MSAR unit is changed into a counter unit. Thus the closed-loop operation is achieved.

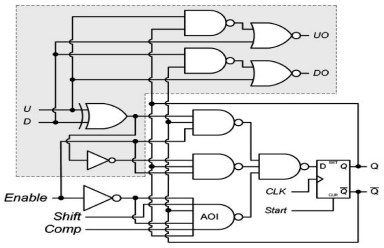

Figure. 7. The implementation of MSAR unit

5. EXPERIMENTAL RESULTS

The SAR-DCC has been made-up in a standard 0.18µm CMOS technology. Fig. 8. shows the planned output clock waveform of the SAR-DCC during the duty-cycle correction process. Within 23 cycles, the output of the DCC is corrected to 50%. Power consumption is measured as 3.2mW.

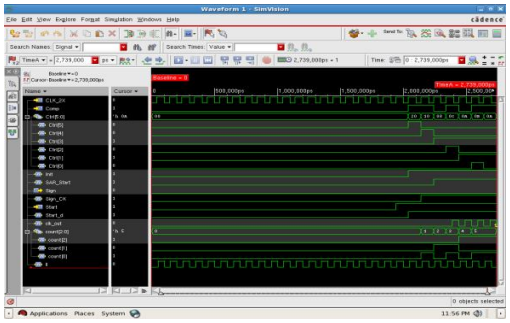

Figure.8. Output of SAR–DCC

The Fig.8 shows the output of SAR – DCC was obtained using Cadence digital lab tool nclaunch.

The model of the MSAR-DCC has been implemented in a standard 0.18µm CMOS technology, by using CADENCE software. The active area is 0.033mm^2. Fig.9. shows the planned output clock waveform of the MSAR-DCC. The output of the DCC is corrected to 50% only within 7 clock cycles and Power consumption is calculated as 5581nW.

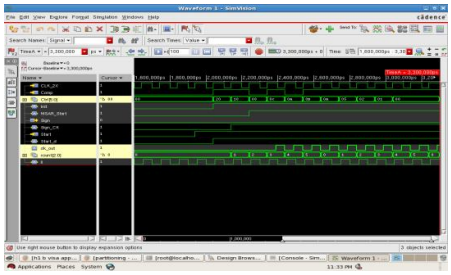

Figure.9 Output of MSAR – DCC

The Fig 9. shows the output of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

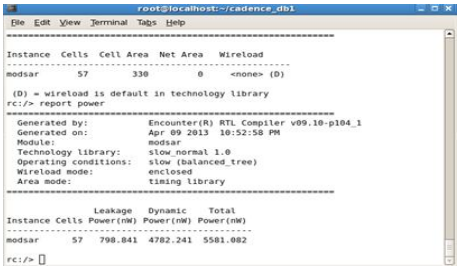

Figure. 10 Power Report of MSAR – DCC

The Fig. 10. shows the Power Report of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

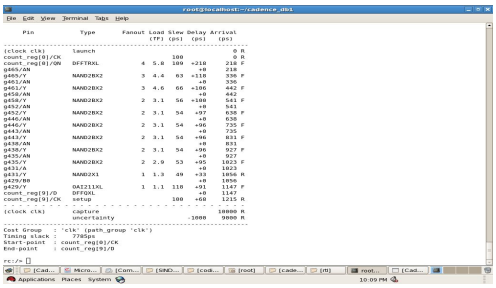

Figure. 11. Timing Report of MSAR – DCC

The Fig 11 shows the Timing Report of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

5.1 Performance Comparison of MSAR – DCC

Performance Comparison of MSAR – DCC

PARAMATERS	**EXISTING SAR – DCC**	**PROPOSED MSAR – DCC**
Architecture	0.18µm	0.18µm
Feedback	Digital feedback DCC	Digital feedback DCC
Correction Time	23 Cycles	7 Cycles
Power	17264.237nW	5581.08nW
Delay Time	1597pS	1214pS
Slew Time	1316pS	930pS

Table 5.1 shows the Performance Comparison result of Modified Successive Approximation Register controlled Duty – Cycle Corrector.

6. CONCLUSION

In this concise, a MSAR-DCC is available. In order to carry out the fastest duty-correction with small die area and to sustain the power-down mode, a MSAR-controller is proposed as a duty-correction controller. Within 7 cycles, the proposed DCC corrects the duty-cycle to 50%. The proposed MSAR-DCC achieves the fastest duty-correction time among feedback type DCCs.

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